IEICE TRANS. ELECTRON., VOL.E96–C, NO.6 JUNE 2013

PAPER Special Section on Analog Circuits and Related SoC Integration Technologies

A 20 GHz Push-Push Voltage-Controlled Oscillator Using Second-Harmonic Peaking Technique for a 60 GHz Frequency Synthesizer*

Teerachot SIRIBURANON[†a)], **Takahiro SATO**[†], **Ahmed MUSA**[†], **Wei DENG**[†], ***Nonmembers***, **Kenichi OKADA**[†], ***Member***, ***and*** **Akira MATSUZAWA**[†], ***Fellow***

SUMMARY This paper presents a 20 GHz push-push VCO realized by a 10 GHz super-harmonic coupled quadrature oscillator for a quadrature 60 GHz frequency synthesizer. The output nodes are peaked by a tunable second harmonic resonator. The proposed VCO is implemented in 65 nm CMOS process. It achieves a tuning range of 3.5 GHz from 16.1 GHz to 19.6 GHz with a phase noise of −106 dBc/Hz at 1 MHz offset. The power consumption of the core oscillators is 10.3 mW and an FoM of −181.3 dBc/Hz is achieved.

key words: *low phase noise, low power, tail-current modulation, impulse sensitivity function, super-harmonic coupled QVCO, push-push VCO*

1. Introduction

To meet the demands for increasing required data rate in future applications, one of the most promising candidates is wireless communication using 60-GHz carrier frequency [1]–[3]. Recently, a high-speed 11-Gb/s wireless communication has been achieved in a 60 GHz CMOS direct-conversion transceiver for IEEE802.15.3c standard [3]. In the design of RF front-ends in the above architecture, one of the most important building blocks is a low-power 60 GHz local oscillator (LO) with quadrature outputs. More importantly, a phase noise, which determines the system performance, of a 60 GHz frequency synthesizer should be less than −90 dBc/Hz at 1 MHz offset for 16QAM modulation scheme [3], [4].

Recently, several architectures for a quadrature 60 GHz generation have been proposed in CMOS technology. Figure 1 shows conventional approaches to generate 60 GHz quadrature signals. The authors in [5] propose a direct 60 GHz quadrature voltage controlled oscillator (QVCO) oscillating at its fundamental frequency as shown in Fig. 1(a). As shown in Fig. 1(b), an alternative solution is proposed in [6] by utilizing a push-push operation of 30 GHz VCO followed by a polyphase filter to generate quadrature signals. In [7], a PLL with a 20 GHz VCO is used as an injection source to a sub-harmonic quadrature Injection Locked Oscillator (ILO) as shown in Fig. 1(c). A calibration system to guarantee a robust operation of ILOs over process-voltage-temperature (PVT) variations has already been demonstrated [8]. Among these publications [5]–[7], only the phase noise of [7] satisfies the requirement for 16QAM modulation which also outperforms [5], [6] in terms of phase noise by more than 20 dB. However, the power consumption of the frequency synthesizer is still high and not suitable for mobile applications. To obtain low phase noise at high frequency, the 20 GHz VCO in [7] consumes significant power consumption comparing to other building blocks. To reduce power consumption of the 20 GHz VCO, this paper proposes a push-push 20 GHz VCO based on a 10 GHz super-harmonic coupled QVCO [9]*. The proposed topology consumes less power consumption while maintaining comparable phase noise performance as in [7].

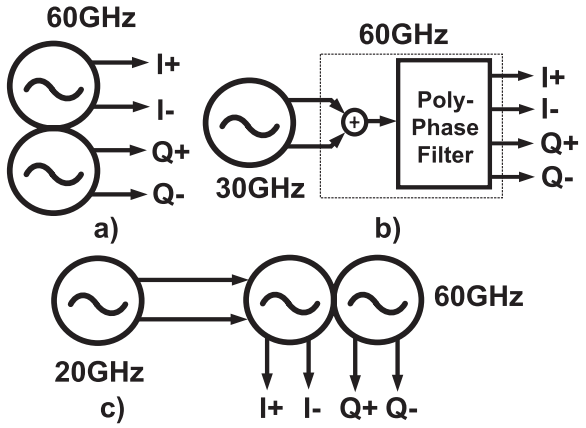


Fig. 1 Conventional approaches for 60 GHz Quadrature LO [5]. (a) 60 GHz QVCO (b) push-push 30 GHz VCO + polyphase filter [6] (c) sub-harmonic 20 GHz VCO + QILO [7].

This paper is organized as followed. An approach to improve a phase noise performance of a 60 GHz frequency synthesizer is proposed and a consideration of overall quality factor of resonator for best VCO performance is discussed in Sect. 2. In Sect. 3, the circuit implementation of the proposed 20 GHz push-push VCO is presented. As well as, the tunable second harmonic resonator and tail modu-

Manuscript received October 29, 2012.
Manuscript revised January 29, 2013.

[†]The authors are with the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, 152-8552 Japan.

*Based on "A 20 GHz Push-Push Voltage-Controlled Oscillator for a 60 GHz Frequency Synthesizer", by T. Siriburanon, T. Sato, A. Musa, W. Deng, K. Okada, A. Matsuzawa which appeared in IEEE Asia-Pacific Microwave Conference 2012 (APMC 2012). © 2012 IEEE.

a) E-mail: tee@ssc.pe.titech.ac.jp

DOI: 10.1587/transele.E96.C.804

lation mechanism is explained. The experimental results and performance comparison with other publications are described in Sect. 4. Finally, a conclusion is summarized in Sect. 5.

2. Design Considerations

2.1 Proposed 60 GHz LO Architecture

An approach for a 60 GHz LO generation is proposed in Fig. 2 by using a push-push 20 GHz VCO in a 20 GHz PLL for 60 GHz sub-harmonic injection. In this case, the main oscillator is running at the half of the desired 20 GHz frequency where the main oscillator can achieve a good quality factor of the tank resonator and relatively higher output power than high-order N-push operation [10]. The second harmonic output of the push-push oscillator can be obtained by connecting I and Q outputs in a push-push configuration since anti-phase fundamental signals will be cancelled out and the second harmonic (20 GHz) signal can be extracted. Main advantages of the proposed VCO over previously-implemented VCOs for 60 GHz signal generations in [5]–[7] are higher achievable quality factor of main resonator tank and less parasitic capacitances, which will be explained in Sect. 2.2. Moreover, the output of main 10 GHz oscillator tank can be used directly to drive a 10 GHz frequency divider where a power-hungry 20 GHz prescaler can be eliminated. Comparing to [7], above merits of this topology are in tradeoffs for a relatively lower output power and a larger area because of the use of the second harmonic and the need of two main oscillator tanks, respectively. The phase noise of the sub-harmonic injection ILO can be estimated by using Eq. (1) where n is a frequency multiplication ratio.

$$PN_{\mathrm{ILO}} = PN_{\mathrm{input}} + 20\log n \quad (1)$$

For 16QAM modulation scheme, phase noise at 60 GHz should be less than −90 dBc/Hz as shown in Table 1. The proposed VCO should provide 10 GHz and 20 GHz signals with a phase noise of less than −105.5 dBc/Hz and −100 dBc/Hz at 1 MHz offset respectively. The tuning range of VCO should cover 9.5–11 GHz for 10 GHz QVCO to cover the whole 7-GHz bandwidth of 60 GHz carrier frequency.

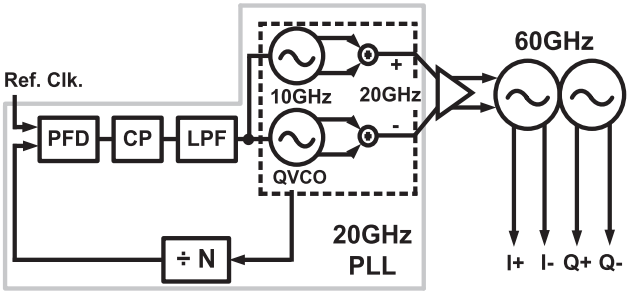


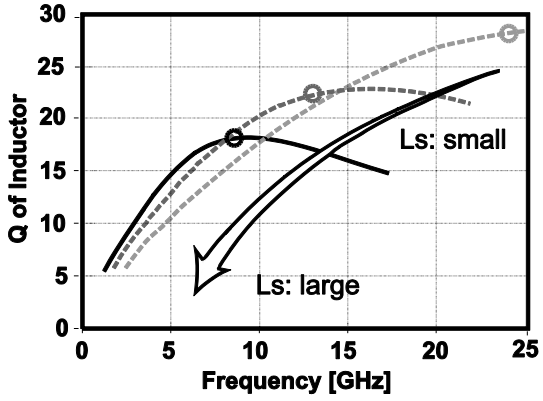
Fig. 2 Proposed 60 GHz Quadrature LO using a 20 GHz push-push VCO (dotted line) in a 20 GHz PLL.

2.2 Optimum Frequency for High Quality Factor of Tank

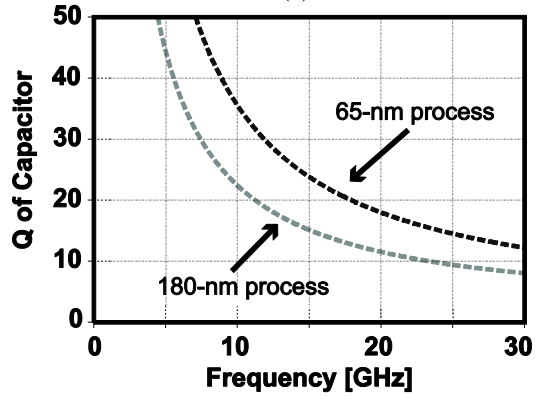
In Fig. 3(a), quality factor of inductor corresponding to

Table 1 Requirements for a VCO in a 60 GHz sub-harmonic injection.

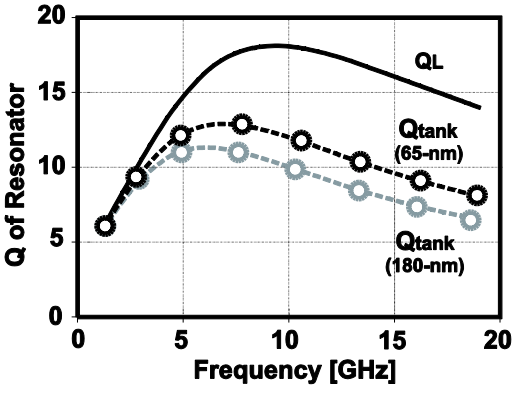
	10GHz	20GHz	60GHz
Phase noise@1MHz offset (dBc/Hz)	-106	-100	-90
Tuning range (GHz)	9.5-11	19-22	57-66



(a)



(b)



(c)

Fig. 3 Quality factor of (a) inductor with various length (b) on-switched capacitors of 65 and 180-nm CMOS process (c) overall tank resonators.

different number of turns of the PDK inductors are plotted. Relatively smaller inductance but higher quality factor can be found in inductor with less number of turns [11]. The quality factor of on-state switched capacitors of 65 nm and 180 nm CMOS process are plotted and compared in Fig. 3(b) based on Eq. (25) and conditions in [12] by keeping the same frequency tuning range, γ, and α to 0.1. Even though maximum quality factor of inductor becomes higher at higher frequencies, the quality factor of on-state switched capacitors is more significant on the performance of VCO at higher frequency as shown in Fig. 3(b). According to the famous Leeson's phase noise equation [13], the phase noise is inversely proportional to the second order of quality factor of the overall tank resonator. From calculation, the quality factor of overall tank resonator is plotted in Fig. 3(c). As a result, the severe degradation of quality factor of turned-on capacitor at high frequency limits the overall quality factor of the resonator tank as the quality factor of resonators in both of dotted lines in Fig. 3(c) fall below 10 at frequency more than 15 GHz. For both technologies, the best overall quality factor of tank in the main oscillator falls in the range from 5–12 GHz. Therefore, a better phase noise performance can be expected in the architecture using a VCO running at frequency around 10 GHz instead of conventional 20 GHz VCO [7] which can be utilized to inject a subharmonic QILO for a 60 GHz signal generation. In addition, due to a better quality factor of turned-on capacitor in 65-nm CMOS process, the overall quality factor of tank resonator is relatively higher than that of the 180-nm CMOS process as shown in Fig. 3(c), which shows that the design of VCO using a more advanced technology can result in a better phase noise performance.

3. Proposed 20 GHz Push-Push VCO Based on 10 GHz Super-Harmonic Coupled QVCO

Conventional cross-coupled 20 GHz VCO has been adopted in [7] but consumes considerable power. Recently, a class-C harmonic VCO which gives more efficient generation of oscillation currents can give significant improvement in VCO performance but reliable start-up issue is still a challenge [14], [15]. In this work, a push-push VCO e.g. [6], [16], [17] is required to allow the main oscillators to run at the desired frequency. A common method is to take a second harmonic output from the common-mode node at different locations e.g. capacitor bank [6], loop ground transmission line [16], virtual ground of a symmetrical inductor [17]. However, these implementations share the same drawback in terms of having a single-ended output. Since differential signals are required for an ILO injection, one possibility is to utilize a quadrature VCO running at half the desired frequency for an extraction of differential push-push signals. A various number of QVCO topologies have been implemented and are realized by two identical LC differential VCOs. Conventionally, quadrature coupling is mainly obtained through two coupling techniques [18] i.e. using coupling transistors [19], [20] and coupling the common-mode nodes of cross-coupled differential pair via a transformer or a direct coupling circuit [21]–[23] known as super-harmonic coupling. While the former suffers from a tradeoff between quadrature accuracy and phase noise, the latter offers a relatively lower-power and lower-phase-noise performance [22], [24]. To the authors' knowledge, this is the first time that a push-push VCO based on super-harmonic coupled QVCO is presented.

3.1 Circuit Implementation

Figure 4(a) shows the circuit schematic of the proposed push-push VCO. It is composed of two NMOS LC VCOs which are super-harmonic coupled at common-mode nodes of the cross-coupled differential pairs via the cross-coupled tail current sources. The cross-coupled tail sources inject a synchronizing signal with strong second harmonic signals enhanced by a tunable second harmonic resonator. PDK inductors with an inductance of 650 pH with a quality factor of 15.7 at 10 GHz are utilized as L_1 and L_2. The size of M1-4 is $2\,\mu\text{m} \times 20$. The tunable second harmonic resonator is composed of an inductor L_3 which has an inductance of 330 pH with a quality factor of 7.9 at 20 GHz, a 2-bit capacitor bank and a varactor as shown in Fig. 4(c). The free-running frequency of the proposed VCO can be tuned through a 3-bit capacitor bank and a varactor of the 10 GHz QVCO for coarse and fine tuning respectively as shown in Fig. 4(b).

Two tail current sources, M5 and M6, with a size of $2\,\mu\text{m} \times 26$, are cross-coupled with the second harmonic resonator that forces the second harmonic at 20 GHz output nodes to be 180 degrees out of phase and further coupling quadrature outputs of fundamental oscillators. In other words, the cross-coupled tail transistors and the second harmonic resonator act as the second harmonic oscillator that is injection locked by the main 10 GHz QVCO. Due to the injection characteristics, the phase noise of 20 GHz output signals will be dependent upon the phase noise of the 10 GHz main oscillator tank and can be derived by Eq. (1) where $n = 2$.

3.2 Tunable Second Harmonic Resonator

Higher amplitudes for both fundamental and second harmonic nodes can be achieved if the tail network is designed to resonate at twice the fundamental frequency as the tail impedance is real, therefore the minimum point of common-node voltage aligns with the minimum point of the fundamental waveforms. As a result, output amplitudes are no longer clamped by common-mode voltage and results in higher amplitudes for both fundamental and second-harmonic outputs [22]. Moreover, it can act as a tail filtering [25] which gives a beneficial effect on phase noise performance. Additionally, a second harmonic resonator helps create an accurate quadrature VCO as reported in [22], [24].

In this proposed circuit, the proposed tunable second harmonic resonator can provide high impedance throughout

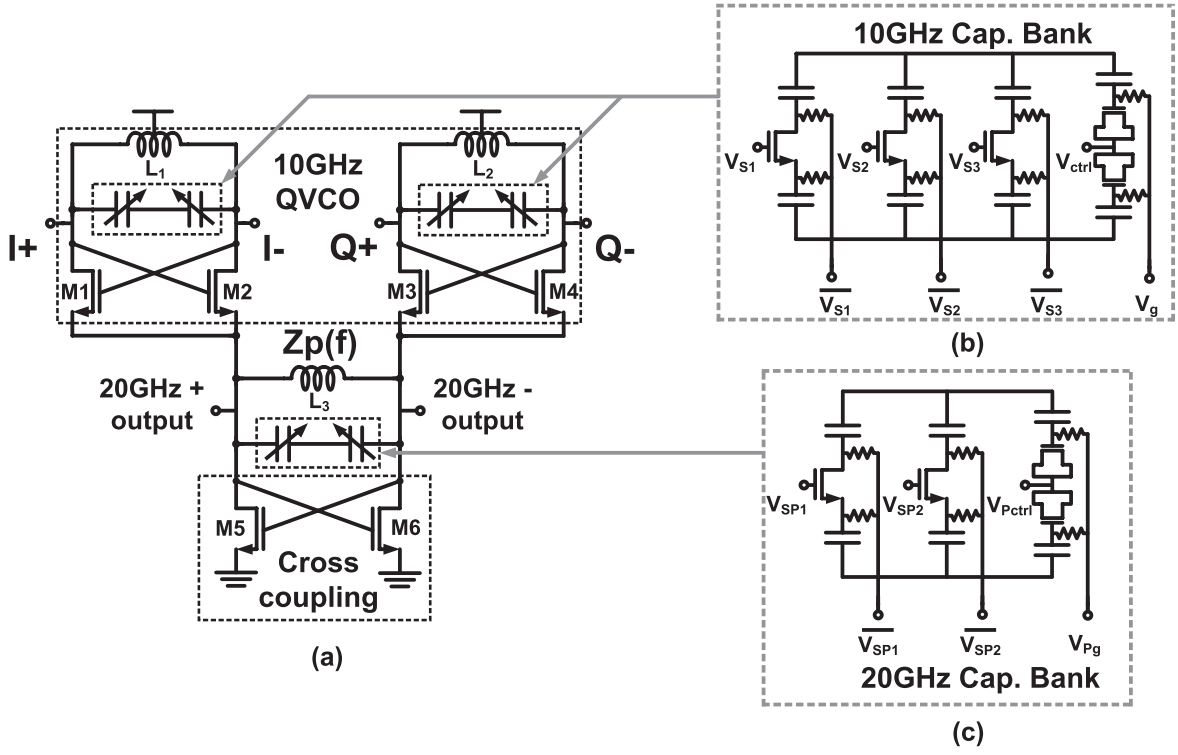


Fig. 4 Schematic of (a) proposed 20 GHz push-push VCO based on 10 GHz subharmonic coupled QVCO with (b) 3-bit capacitor bank for a 10 GHz resonator (c) 2-bit capacitor bank for a 20 GHz resonator.

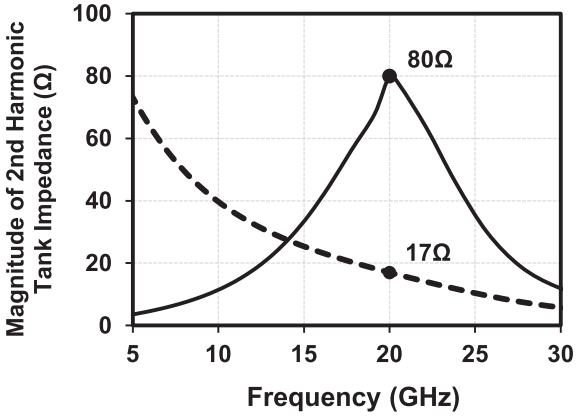


Fig. 5 Comparison of the simulated magnitude of the 2nd harmonic tank impedance versus frequency with (solid line) and without (dotted line) the proposed tunable second harmonic resonator.

the tuning range. The inductor L_3 is placed across the second harmonic resonator which resonates with parasitic capacitance of cross-coupled pair of fundamental oscillators, equivalent capacitance from a varactor and a 2-bit capacitor bank. Figure 5 shows the magnitude of second harmonic tank impedance of the VCO with and without the proposed second harmonic resonator. Note that the VCO without the second harmonic resonator is composed of the tail cross coupled pair in parallel with the 20 GHz output nodes. The inductor in the second harmonic resonator resonates with a variable capacitor and a tail cross-coupled pair. Hence, it boosts the impedance seen at output nodes by a factor of 4.7 at twice the fundamental frequency from 17 Ω to 80 Ω as shown in Fig. 5. From simulation, the average of output amplitude over the entire tuning range of the 20 GHz output in the case with the tunable second harmonic resonator is approximately 57% (200 mV) higher than the case without the proposed resonator as shown in Fig. 6. Consequently, this allows oscillation swing of the main 10 GHz oscillators of the proposed work to increase over the case without second harmonic resonator and improve the phase noise performance of the 10 GHz main oscillator as shown in Fig. 7. This is beneficial to the phase noise of 20 GHz outputs according to injection-locked characteristics Eq. (1).

3.3 Tail Modulation Mechanism

An improvement in phase noise performance can also be described in terms of current modulation of the tail transistors and the impulse sensitivity function (ISF) of the fundamental waveforms. Wavesforms in Fig. 8(b) show the 10 GHz waveforms of the main tank I located on the left side as shown in Fig. 8(a) and its ISF which is approximated by taking the derivative of the waveforms of fundamental freqeuncy. The third waveform is a waveform at the common-mode node of the main tank Q which is an input to the tail current source of the I-tank VCO. The bottom waveform shows the waveform of modulated current of tail transis-

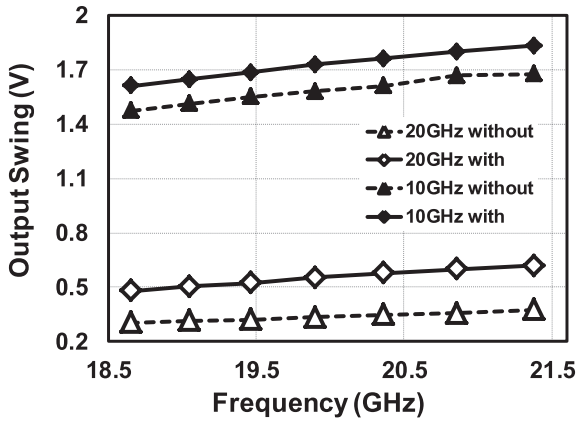


Fig. 6 Simulated output swings of 20 GHz and 10 GHz of the VCO with and without the proposed tunable second harmonic resonator.

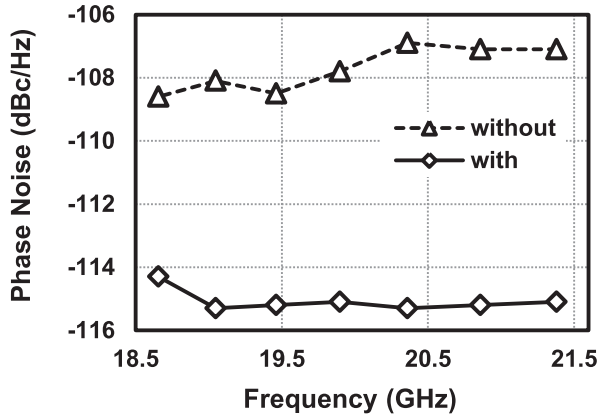


Fig. 7 Simulated phase noise of the 10 GHz main VCO with and without the proposed tunable second harmonic resonator.

tor M5 that inject the current into the tank of fundamental oscillator I.

Providing that the second harmonic resonator is resonated at exactly twice the fundamental frequency via tunable switches, the corresponding waveforms can be aligned and illustrated as shown in Fig. 8(b). The second harmonic output waveform at the common-mode node of tank-Q resonator is input and conducts the highest amplitude of current waveform (I_{bias}) at its highest amplitude. The modulated current is maximized during the period where the ISF is at its minimum and minimized during the period where the ISF is at its maximum. Therefore, this can alleviate the noise injection to the tank and the phase noise performance can be improved.

4. Experimental Results

The proposed 20 GHz push-push VCO using second-harmonic peaking technique (Fig. 4) is fabricated in a 12-metal 65-nm CMOS process. A die photo is shown in Fig. 9 in which the core VCO occupies an area of 570 μm $\times$ 490 μm. The phase noise is evaluated by using a signal source analyzer (Agilent E5052B). Through 8 bands

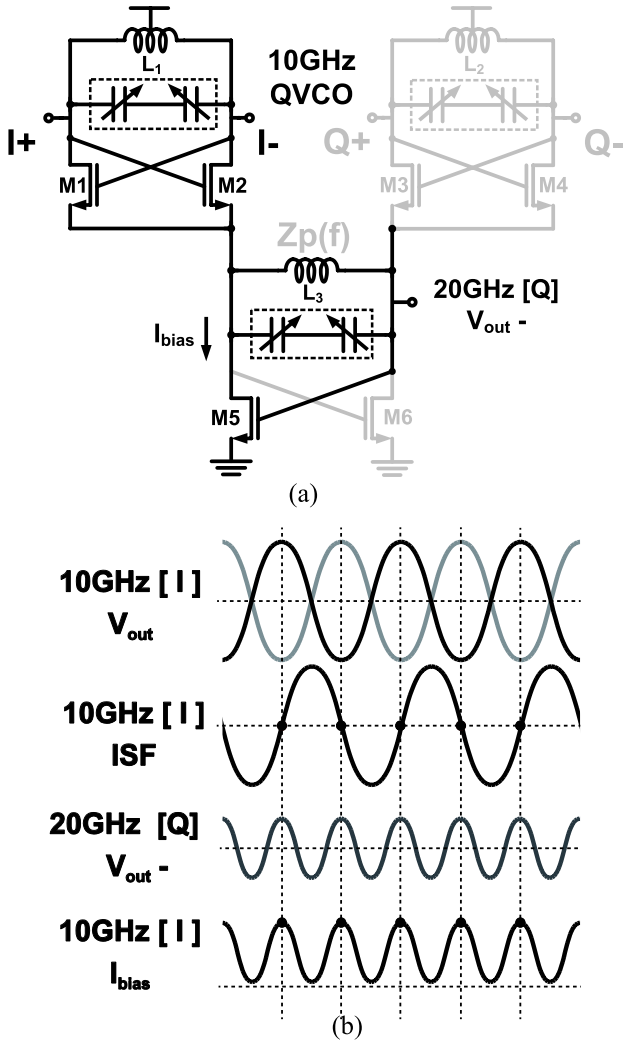


Fig. 8 Circuit schematic of the oscillator tank I (a) and its corresponding waveforms (b) for illustration of tail modulation mechanism.

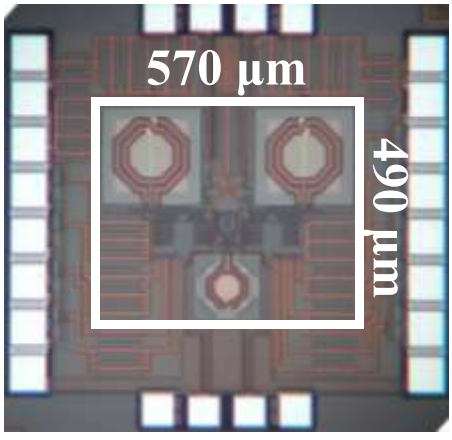


Fig. 9 Die photo of the proposed 20 GHz push-push VCO.

of the 3-bit switched capacitor of the fundamental oscillator, the proposed VCO can operate from 16.1–19.6 GHz (19.6% tuning range). The tuning range of each band is

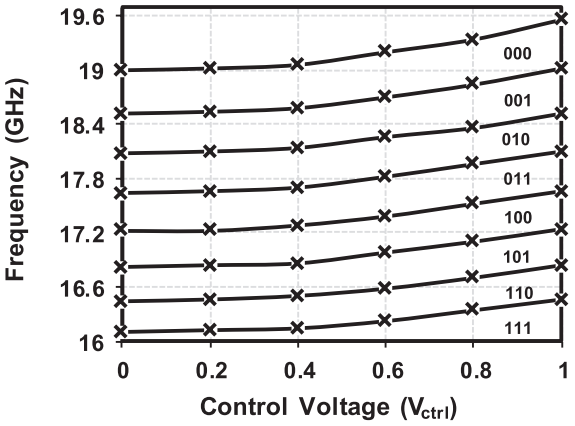


Fig. 10 Measured tuning range with its corresponding 3-bit switch codes (V_{S3}, V_{S2}, V_{S1}).

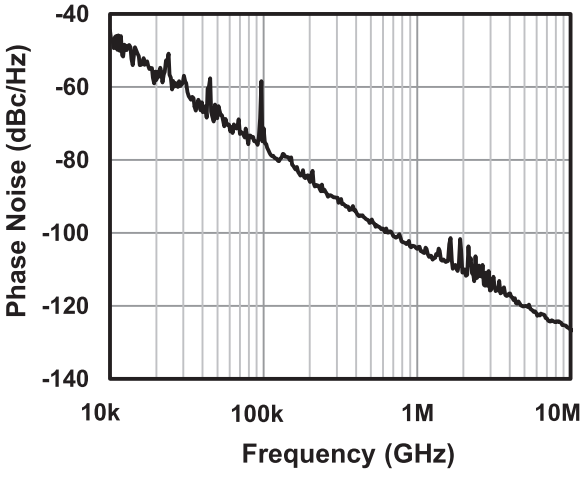


Fig. 11 Measured phase noise at 18.8 GHz.

shown in Fig. 10. Despite a satisfying tuning range, the measured operating frequency of the proposed VCO considerably drops. Consequently, the proposed VCO, if used for 60 GHz subharmonic injection, cannot cover the desired 60 GHz band. The measured phase noise at 18.8 GHz is −106 dBc/Hz at 1 MHz offset as shown in Fig. 11. In this work, the second harmonic resonator is manually tuned to make the impedance peak at the frequency in the vicinity of two times oscillation frequency of main 10 GHz oscillators to achieve an optimum phase noise performance. Figure 12 shows a phase noise of 20 GHz output from different (V_{SP1}, V_{SP2}) and V_{Pctrl} of the tunable second harmonic resonator. The phase noise slightly degrades if the peak impedance of 20 GHz resonator is in the vicinity of twice the oscillation frequency of the main oscillator as shown in Fig. 12. The Figure of Merit (FoM) is defined as:

$$FoM = L(f_{\text{offset}}) - 20\log\left(\frac{f_o}{f_{\text{offset}}}\right) + 10\log\left(\frac{P_{\text{DC}}}{1\text{mW}}\right) \quad (2)$$

where $L(f_{\text{offset}})$ is phase noise, f_{offset} is offset frequency, f_0 is oscillation frequency and P_{DC} is power consumption. The FoM of the proposed VCO is −181.3 dBc/Hz. Two-stage

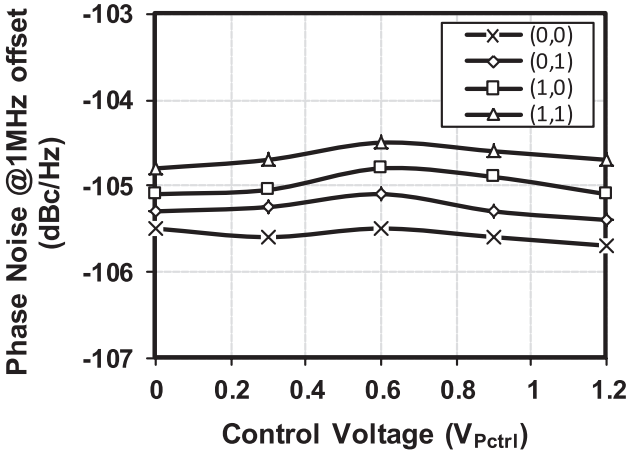


Fig. 12 Measured phase noise of 20 GHz output from different (V_{SP1}, V_{SP2}) and V_{Pctrl} of the tunable second harmonic resonator while V_{Pg} = 0.6 V.

common source buffers are used to isolate the output port with the measurement equipment so that it does not directly load the tank and does not degrade the performance. Due to unmatched output port of the buffer with 50 ohm characteristic of the measurement equipment and further loss from cable and connectors, a measured 20 GHz output power of −28 dBm is observed. To approximate output power after the buffer, a simulation has been performed by including the effect of 50 ohm impedance at output of the buffer to represent the characteristic of the measurement equipment. The output power after the buffer is 130 mV which is approximately −14 dBm. Since loss from measurement equipment is at least 10 dB, the approximated output power is −24 dBm which is close to the measured output power. From 1.1-V supply, the proposed oscillator consumes only 10.3 mW of power.

Table 2 compares the performance of the proposed VCO with previously-implemented VCOs that is used for 60 GHz generations [5]–[7] and other 20 GHz VCOs [26]–[28]. Due to the degradation of the quality factor of the overall tank at high frequency as explained in Sect. 2.2, an approach in [5] and [6] using a direct 60 GHz QVCO and a push-push VCO based on 30 GHz fundamental oscillator suffered from high phase noise. As a result of less impact of the parasitic capacitance, an approach which is based on a 20 GHz VCO [7] has improved the phase noise performance by a reduction of −20 dBc/Hz comparing to [5], [6]. Due to a possibility of achieving a better VCO performance, the main oscillator is chosen to operate at frequency where quality factor of resonator tank can be maximized as suggested in Fig. 3(c). Therefore, in this proposed work, a push-push 20 GHz VCO based on 10 GHz super-harmonic coupled QVCO is implemented. As a result, the proposed VCO consumes only 10.3 mW while achieving equivalent phase noise performance as the previously implemented 20 GHz VCO in [7]. Consequently, it shows approximately 2 dB improvement in FoM. The performance of the proposed VCO also shows a competitive performance with the state-of-the-

Table 2 Performance comparison.

	Features	CMOS Tech.	Frequency [GHz]	Phase noise [dBc/Hz]	Power [mW]	FoM [dBc/Hz]	Output type
[5]	QVCO@60GHz	45nm	57-66	-75@1MHz	28.8	-156.8	Quad.
	Direct 60GHz QPLL	45nm	57-66	-75@1MHz	78	-	Quad.
[6]	Push-push VCO@30GHz	90nm	29.8-32	-79@1MHz	9.8	-159.2	Diff.
	VCO + Polyphase filter	90nm	59.6-64	-73@1MHz	76	-	Quad.
[7]	VCO@20GHz	65nm	17.9-21.2	-106@1MHz	19	-179	Diff.
	Sub-harmonic Injection	65nm	58-63	-96@1MHz	80	-	Quad.
[26]	CMOS VCO @20GHz	180nm	20-21.5	-102@1MHz	45	-172	Diff.
[27]	Capacitive feedback VCO @20GHz	180nm	19.7-20.2	-111@1MHz	32	-181.9	Diff.
[28]	Current Reuse VCO + Tripler	180nm	21.1-24.9	-105@1MHz	9	-182	Diff.
This work	Push-push VCO@10GHz	65nm	16.1-19.6	-106@1MHz	10.3	-181.3	Diff.
	Sub-harmonic Injection (based on calculation)	65nm	48.3-58.8	-96@1MHz	-	-	Quad.

art 20 GHz VCOs in [27], [28].

A phase noise performance of the proposed push-push VCO in a 20 GHz PLL for a sub-harmonic injection ILO can be approximately calculated by Eq. (1) where $n = 3$ for a third-order harmonic ILO as implemented in [5]. Based on calculation, if the proposed 20 GHz push-push VCO is implemented in [7], a phase noise of approximately −96 dBc/Hz can be achieved, which satisfies the requirement for 16QAM modulation scheme and considerably better than the phase noise performance in [5], [6].

5. Conclusion

This paper discusses a consideration of architectures for low-phase noise high-performance 60 GHz frequency synthesizer. From the consideration of limit of quality factor of the overall resonator tank, a proposed 20 GHz push-push VCO based on a 10 GHz super-harmonic coupled QVCO achieves an improvement of 2.3 dB in FoM over the previously-implemented 20 GHz VCO [7] and has a competitive performance compared to the-state-of-the-art 20 GHz VCOs [27], [28]. The proposed VCO can be utilized in a 20 GHz PLL for a sub-harmonic injection to an ILO. Based on calculation, the 60 GHz frequency synthesizer which utilizes the proposed push-push VCO can satisfy the requirement for 16QAM modulation scheme.

Acknowledgments

This work was partially supported by MIC, SCOPE, MEXT, STARC, NEDO, Canon Foundation, and VDEC in collaboration with Cadence Design System, Inc., and Agilent Technologies Japan. Ltd.

References

[1] K. Okada, K. Kondou, M. Miyahara, M. Shinagawa, H. Asada, R. Minami, T. Yamaguchi, A. Musa, Y. Tsukui, Y. Asakura, S. Tamonoki, H. Yamagishi, Y. Hino, T. Sato, H. Sakaguchi, N. Shimasaki, T. Ito, Y. Takeuchi, N. Li, Q. Bu, R. Murakami, K. Bunsen, K. Matsushita, M. Noda, and A. Matsuzawa, "A full 4-channel 6.3 Gb/s 60 GHz direct-conversion transceiver with low-power analog and digital baseband circuitry," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp.218–220, Feb. 2012.

[2] K. Okada, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, N. Li, S. Ito, W. Chaivipas, R. Minami, and A. Matsuzawa, "A 60 GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE 802.15.3c," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp.160–162, Feb. 2011.

[3] K. Okada, N. Li, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, S. Ito, W. Chaivipas, R. Minami, T. Yamaguchi, Y. Takeuchi, H. Yamagishi, M. Noda, and A. Matsuzawa, "A 60-GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE802.15.3c," IEEE J. Solid-State Circuits, vol.46, no.12, pp.2988–3004, Dec. 2011.

[4] B.A. Floyd, "A 16–18.8-GHz sub-integer-N frequency synthesizer for 60-GHz transceivers," IEEE J. Solid-State Circuits, vol.43, no.5, pp.1076–1086, May 2008.

[5] K. Scheir, G. Vandersteen, Y. Rolain, and P. Wambacq, "A 57-to-66 GHz quadrature PLL in 45 nm digital CMOS," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp.494–495, 495a, Feb. 2009.

[6] C. Marcu, D. Chowdhury, C. Thakkar, J.-D. Park, L.-K. Kong, M. Tabesh, Y. Wang, B. Afshar, A. Gupta, A. Arbabian, S. Gambini, R. Zamani, E. Alon, and A.M. Niknejad, "A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry," IEEE J. Solid-State Circuits, vol.44, no.12, pp.3434–3447, Dec. 2009.

[7] A. Musa, R. Murakami, T. Sato, W. Chaivipas, K. Okada, and A. Matsuzawa, "A low phase noise quadrature injection locked frequency synthesizer for MM-wave applications," IEEE J. Solid-State Circuits, vol.46, no.11, pp.2635–2649, Nov. 2011.

[8] W. Deng, T. Siriburanon, A. Musa, K. Okada, and A. Matsuzawa, "A 58.1-to-65.0 GHz frequency synthesizer with background calibration for millimeter-wave TDD transceivers," IEEE European Solid-State Circuits Conference (ESSCIRC), pp.201–204, Sept. 2012.

[9] T. Siriburanon, T. Sato, A. Musa, W. Deng, K. Okada, and A. Matsuzawa, "A 20 GHz push-push voltage-controlled oscillator for a 60 GHz frequency synthesizer," IEEE Asia-Pacific Microwave Conference (APMC), Kaohsiung, Taiwan, Dec. 2012.

[10] A. Musa, K. Okada, and A. Matsuzawa, "A 20 GHz ILFD with locking range of 31% for divide-by-4 and 15% for divide-by-8 using progressive mixing," IEEE Asian Solid State Circuits Conference

(A-SSCC), pp.85–88, Nov. 2011.
[11] S. Hara, T. Ito, K. Okada, and A. Matsuzawa, "Design space exploration of low-phase-noise LC-VCO using multiple-divide technique," IEEE International Symposium on Circuits and Systems (ISCAS), pp.1966–1969, May 2008.
[12] R. Murakami, S. Hara, K. Okada, and A. Matsuzawa, "Design optimization of voltage controlled oscillators in consideration of parasitic capacitance," IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp.1010–1013, Aug. 2009.
[13] D.B. Leeson, "A simple model of feedback oscillator noise spectrum," Proc. IEEE, vol.54, no.2, pp.329–330, Feb. 1966.
[14] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," IEEE J. Solid-State Circuits, vol.43, no.12, pp.2716–2729, Dec. 2008.
[15] W. Deng, K. Okada, and A. Matsuzawa, "A feedback class-C VCO with robust startup condition over PVT variations and enhanced oscillation swing," IEEE European Solid-State Circuits Conference (ESSCIRC), pp.499–502, 2011.
[16] T. Nakamura, T. Masuda, K. Washio, and H. Kondoh, "A push-push VCO with 13.9-GHz wide tuning range using loop-ground transmission line for full-band 60-GHz transceiver," IEEE J. Solid-State Circuits, vol.47, no.6, pp.1267–1277, June 2012.
[17] E. Seok, D. Shim, C. Mao, R. Han, S. Sankaran, C. Cao, W. Knap, and K.O. Kenneth, "Progress and challenges towards terahertz CMOS integrated circuits," IEEE J. Solid-State Circuits, vol.45, no.8, pp.1554–1564, Aug. 2010.
[18] A. Buonomo, M.P. Kennedy, and A. Lo Schiavo, "On the synchronization condition for superharmonic coupled QVCOs," IEEE Trans. Circuits Syst. I: Regular Papers, vol.58, no.7, pp.1637–1646, July 2011.
[19] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900 MHz CMOS LC-oscillator with quadrature outputs," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp.392–393, Feb. 1996.
[20] P. Andreani, A. Bonfanti, L. Romano, and D. Samori, "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," IEEE J. Solid-State Circuits, vol.37, no.12, pp.1737–1747, Dec. 2002.
[21] J. Cabanillas, L. Dussopt, J.M. Lopez-Villegas, and G.M. Rebeiz, "A 900 MHz low phase noise CMOS quadrature oscillator," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp.63–66, 2002.
[22] S.L.J. Gierkink, S. Levantino, R.C. Frye, C. Samori, and V. Boccuzzi, "A low-phase-noise 5-GHz CMOS quadrature VCO using superharmonic coupling," IEEE J. Solid-State Circuits, vol.38, no.7, pp.1148–1154, July 2003.
[23] T.M. Hancock and G.M. Rebeiz, "A novel superharmonic coupling topology for quadrature oscillator design at 6 GHz," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp.285–288, June 2004.
[24] I.R. Chamas and S. Raman, "Analysis and design of a CMOS phase-tunable injection-coupled LC quadrature VCO (PTIC-QVCO)," IEEE J. Solid-State Circuits, vol.44, no.3, pp.784–796, March 2009.
[25] E. Hegazi, H. Sjöland, and A.A. Abidi, "A filtering technique to lower LC oscillator phase noise," IEEE J. Solid-State Circuits, vol.36, no.12, pp.1921–1930, Dec. 2001.
[26] D. Ozis, N.M. Neihart, and D.J. Allstot, "Differential VCO and passive frequency doubler in 0.18 m CMOS for 24 GHz applications," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp.45–48, June 2006.
[27] H.-H. Hsieh and L.-H. Lu, "A low-phase-noise κ-band CMOS VCO," IEEE Microw. Wireless Compon. Lett., vol.16, no.10, pp.552–554, Oct. 2006.
[28] P.-K. Tsai and T.-H. Huang, "Integration of current-reused VCO and frequency tripler for 24-GHz low-power phase-locked loop applications," IEEE Trans. Circuits Syst. II: Express Briefs, vol.59, no.4, pp.199–203, April 2012.

Teerachot Siriburanon received the B.E. in Telecommunications from Sirindhorn International Institute of Technology (SIIT), Thammasat University, Thailand and the M.E. in Physical Electronics from Tokyo Institute of Technology, Japan in 2010 and 2012, respectively. He is currently pursuing the Ph.D. degree in Physical Electronics at Tokyo Institute of Technology, Japan. His research interests are CMOS RF/millimeter-wave transceiver systems and clock/frequency generations for wireless and wireline communications.

Takahiro Sato received the B.E. degree in electrical and electronic engineering in 2010 and M.E. degree in physical electronics in 2012 from Tokyo Institute of Technology, Tokyo, Japan. He is currently with Nintendo, Japan.

Ahmed Musa received both B.Sc. degrees in electrical engineering and computer engineering from King Fahd University of Petroleum and Minerals (KFUPM), Dhahran, KSA, in 2006, and the M.S. degree in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2009. He is currently pursuing the Ph.D. degree in physical electronics at Tokyo Institute of Technology, Japan. His research interests are CMOS RF/microwave circuit design and PLL frequency synthesizers. Mr. Musa received the ASP-DAC Special Feature Award in 2011.

Wei Deng received the B.S. and M.S. degrees from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2006 and 2009, respectively. Currently, he is working toward Ph.D. degree at Tokyo Institute of Technology, Tokyo, Japan. His research interests include analog/RF/millimeter-wave transceiver systems and clock/frequency generation systems for wireline and wireless communications. He was the recipient of the ISSCC Travel Grant Award in 2010, the Honor Scholarship from 2010 to 2013, the Excellent Student Award at Tokyo Institute of Technology in 2011, the China Youth Science and Technology Innovation Award in 2011, the IEEE Solid-State Circuits Society Predoctoral Achievement Award in 2012, the Chinese Government Award for Outstanding Self-financed (non-government sponsored) Students Abroad in 2013, and the Seiichi Tejima Overseas-Student Research Award in 2013. He is a technical reviewer for several international journals and conferences.

Kenichi Okada received the B.E., M.E. and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively. From 2000 to 2003, he was a Research Fellow of the Japan Society for the Promotion of Science in Kyoto University. From 2003 to 2007, he worked as an Assistant Professor at Precision and Intelligence Laboratory, Tokyo Institute of Technology, Yokohama, Japan. Since 2007, he has been an Associate Professor at Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan. He has authored or co-authored more than 200 journal and conference papers. His current research interests include reconfigurable RF CMOS circuits for millimeter-wave CMOS wireless frontends, cognitive radios, and low-voltage RF circuits. He is a member of IEEE, the Information Processing Society of Japan (IPSJ), and the Japan Society of Applied Physics (JSAP). He received the Ericsson Young Scientist Award in 2004, the A-SSCC Outstanding Design Award in 2006 and 2011, the ASP-DAC Special Feature Award in 2011, and 32 international and domestic awards. He is a member of the ISSCC Technical Program Committee.

Akira Matsuzawa received B.S., M.S., and Ph.D. degrees in electronics engineering from Tohoku University, Sendai, Japan, in 1976, 1978, and 1997 respectively. In 1978, he joined Matsushita Electric Industrial Co., Ltd. Since then, he has been working on research and development of analog and Mixed Signal LSI technologies; ultra-high speed ADCs, intelligent CMOS sensors, RF CMOS circuits, and digital read-channel technologies for DVD systems. He was also responsible for the development of low power LSI technology and SOI devices. From 1997 to 2003, he was a general manager in advanced LSI technology development center. On April 2003, he joined Tokyo Institute of Technology and he is professor on physical electronics. Currently he is researching in mixed signal technologies; RF CMOS circuit design for SDR and high speed and ultra-low power data converters. He served a guest editor in chief for special issue on analog LSI technology of IEICE transactions on electronics in 1992, 1997, and 2003, and committee member for analog technology in ISSCC. Recently he served IEEE SSCS elected Adcom and IEEE SSCS Distinguished lecturer. Now he serves chapter chair of IEEE SSCS Japan Chapter and vice president of Japan Institution of Electronics Packaging. He received the IR 100 award in 1983, the R&D 100 award and the remarkable invention award in 1997, and the ISSCC evening panel award in 2003 and 2005. He is an IEEE Fellow since 2002, and an IEICE Fellow since 2010.